DELAY-LOCKED-LOOP (DLL) HAVING SYMMETRICAL RISING AND FALLING CLOCK EDGE TYPE DELAYS

Abstract of the Disclosure

A circuit and method are provided wherein a receiver receives an input train of pulses. The circuit includes a delay-locked-loop coupled to an output of the receiver. The delay-locked-loop includes a pulse generator responsive to received input train of pulses produced at the output of the receiver for producing first pulses in response to the leading edges of the received input train of pulses and second pulses in response to the trailing edges of received input train of pulses. The leading edge of the first pulse has the same edge type as the leading edge of the second pulse (i.e., the leading edge of the first pulse and the leading edge of the second pulse are either both rising edge types or both falling edges types). The first pulses and the second pulses are combined into a composite input signal comprising the first and second pulses with the leading edge of the first pulse maintaining the same edge type. The delay-locked-loop also includes a variable delay line fed by the composite input signal for producing a composite output train of pulses comprising both the first train of pulses and the second train of pulses after a selected time delay provided by the delay line. The delay-locked-loop is responsive to one of the first train of pulses and the second train of pulses in the composite output train of pulses for selecting the time delay of the variable delay line so as to produce the composite output train of pulses with a predetermined phase relationship to the input train of pulses.